Improved Computer-Aided Synthesis Tools for the Design of Matching Networks for Wide-Band Microwave Amplifiers

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Abstract—**Network synthesis is a powerful design tool when applied to the design of matching networks for wide-band microwave amplifiers. Significant design improvements have been made in the computer-aided synthesis process, which provides a powerful, efficient, and friendly tool for the microwave amplifier designer. Design methodologies are given, computer automation methods are outlined, and a complete amplifier design example is included.**

I. Introduction

NETWORK SYNTHESIS has long been a workhorse tool for the design of low-frequency and microwave filters. In recent years, it has begun to be applied to the problem of wide-band matching networks for microwave amplifiers [1], [2] via extensions of classical synthesis techniques. This paper describes significant improvements in the synthesis of matching networks for wide-band amplifiers and in the automation thereof. The key improvements are 1) a simplified and automated method of modeling device impedances; 2) an efficiently automated methodology for selecting topologies that meet parasitic inclusion and impedance transformation requirements; and 3) an automated method for adjusting the gain–bandwidth and selecting reflection coefficient zeros consistent with parasitics to be included. These improvements provide a powerful, friendly, and useful tool for the microwave amplifier designer.

In Section II, the synthesis design process as applied to wide-band matching networks is outlined, with attention called to the steps which have been significantly improved via the techniques described in this paper.

Sections III, IV, and V describe in detail the areas of improved design methods in the matching network synthesis process.

Sections VI and VII describe complete microwave amplifier designs using the design techniques of this paper.

Section VIII summarizes the results and benefits possible using the design methodologies of this paper.

II. Steps in the Matching Network Synthesis Process

The steps in matching network synthesis are outlined in Fig. 1 and listed here. Steps shown with an (*) indicate areas in which significant improvements have been made via the techniques described in the following sections.

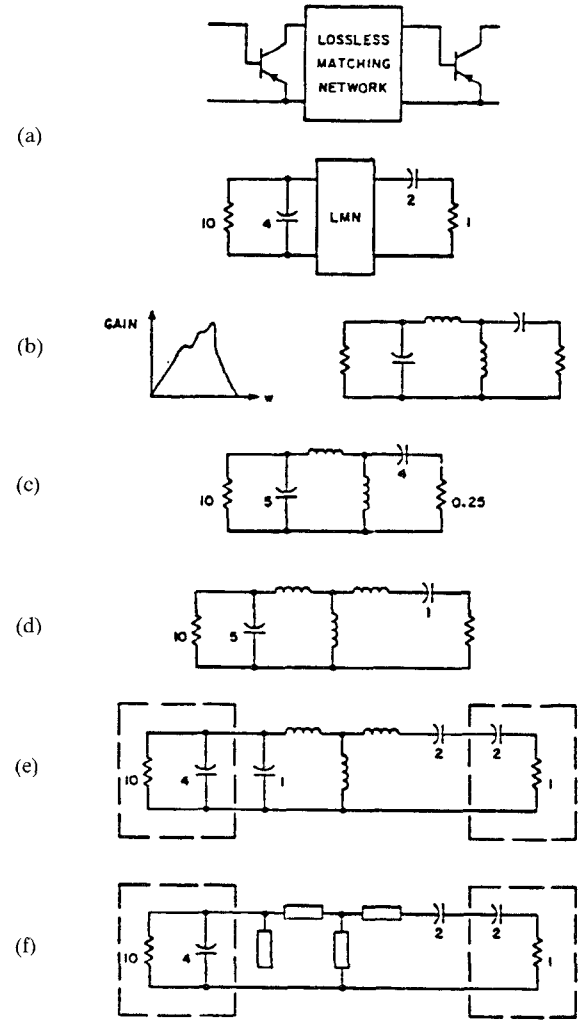

Fig. 1. Outline of the process of synthesis of matching networks for microwave amplifiers. (a) Model device impedances. (b) Constrain frequency response and select topology consistent with parasitic elements. Select reflection coefficient zeros. (c) Synthesize network. (d) Transform impedance. (e) Separate out device impedances. (f) Transform design to approximated transmission-line equivalent.

*1) Model the input and output impedance of the active devices to be used in the microwave amplifier.

*2) Select a topology consistent with device parasitics.

*3) Adjust the gain–bandwidth to insure inclusion of parasitics.

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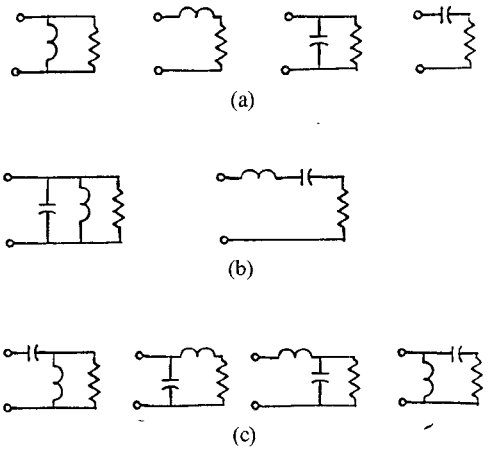

Fig. 2. Simple impedance models for modeling active device impedances. (a) Two-element models. (b) Three-element series–series or shunt models. (c) Three-element shunt–series models.

*4) Select the reflection coefficient zeros consistent with inclusion of parasitics.

5) Transform impedances to desired levels.

6) Transform the lumped design to a transmission-line realization.

7) Analyze the resultant design by itself and/or as part of the complete amplifier design.

8) Optimize the amplifier design (if needed).

III. A Simplified and Automated Method of Modeling Device Impedances

Historically, the input and output impedances of active devices have generally been modeled by curve-fitting, optimization, or Smith chart manipulation. More recently, algebraic solutions for topologies of cascaded resonant circuits have been developed [3]. An algebraic method is developed here to fit two- and three-element models to measured data. These models are not restricted to be cascades of resonant circuits, and therefore have the potential of yielding simpler impedance models. This method provides very satisfactory accuracy and greatly improved speed and convenience by using the simple impedance models shown in Fig. 2. The modeled element values are then obtained by applying the following constraints to the three different types of circuits.

Circuit Type	*Constraint at f_u (upper passband edge)*	*Constraint at f_l (lower passband edge)*
Two-Element Networks	Exact agreement with measured impedance: both real and imaginary parts	None
Three-Element Series–Series or Shunt–Shunt type	Exact agreement of both real and imaginary parts	Agreement of imaginary parts
Three-Element Series–Shunt Type	Exact agreement of both real and imaginary parts	Agreement of real parts

Then the behavior of the model at f_l is compared to the device impedance from measured S-parameters. From the networks which yield a realizable network, the impedance model which has the greatest accuracy at f_l is chosen. The degree of accuracy of the model at f_l is obtained by simply computing the resultant model behavior at f_l, comparing to the actual Z behavior at f_l, and computing the potential matching error due to modeling inaccuracy. The worst-case modeling error under conjugate matching is used as an error criterion.

This method yields very accurate results with quite simple models. An application example is given with the amplifier designs of Sections VI and VII.

A representative derivation of the modeling equations will be given for each type of network; then all of the design equations will be summarized. In fitting the circuit models to measured data, the following impedance and admittance definitions are used for all models:

Measured Impedance

$$Z = \frac{(1+S_{ii})Z_0}{(1-S_{ii})}, \qquad \begin{matrix} i=1 \text{ for input} \\ i=2 \text{ for output} \end{matrix} \tag{1}$$

$$Z = R_u + jX_u = \frac{1}{G_u + jB_u}, \qquad f = f_u \tag{2}$$

$$Z = R_l + jX_l = \frac{1}{G_l + jB_l}, \qquad f = f_l. \tag{3}$$

A. Two-Element Modeling: Representative Equation Derivation

The modeling equations for the series C, R (see Fig. 2(a)) circuit are easily obtained by requiring exact agreement of the model at $f = f_u$.

$$R = R_u \tag{4}$$

$$C = -1/(2\pi f_u X_u). \tag{5}$$

B. Three-Element Series–Series or Shunt–Shunt Models: Representative Equation Derivation

Equations for the shunt L, shunt C, R circuit (see Fig. 2(b)) are obtained by first setting the real parts of the admittance equal at $f = f_u$

$$R = 1/G_u. \tag{6}$$

Further, setting the imaginary parts equal at f_u yields the following equation:

$$B_u = 2\pi f_u C - 1/(2\pi f_u L). \tag{7}$$

We need one more constraint to determine C and L. We could choose to set either the real or the imaginary parts equal at $f = f_l$. In this particular model, however, the real part of the admittance is already determined by (6)

$$G_l = G_u = 1/R. \tag{8}$$

We therefore choose to set the imaginary part of the model equal to measured parameters at f_l:

$$B_l = 2\pi f_l C - 1/(2\pi f_l L). \tag{9}$$

If (7) is multiplied by f_u/f_l and added to (9), the result is

$$B_u(f_u/f_l) - B_l = 2\pi C(f_u^2/f_l - f_l)$$

or

$$C = [B_u f_u/f_l - B_l]/[f_u^2/f_l - f_l]/(2\pi). \tag{10}$$

Since (10) provides a value for C, L can now be obtained

by using this known C in (7)

$$L = 1/(2\pi f_u C - B_u)/(2\pi f_u). \tag{11}$$

Equations (6), (10), and (11) give the design values for R, C, and L. Note that, depending on the measured data, negative elements may result from these equations and can be discarded in favor of other realizable circuit models.

C. Three-Element Models of the Series–Shunt or the Shunt–Series Type: Representative Equation Derivation

For the shunt C, series L, R model (see Fig. 2(c)), we first set the real and imaginary parts of the admittance equal to measured data at $f = f_u$:

real parts equal = = >

$$G_u = R/\left[R^2 + (2\pi f_u L)^2\right] \tag{12}$$

imaginary parts equal = = >

$$B_u = 2\pi f_u C - (2\pi f_u L)/\left[R^2 + (2\pi f_u L)^2\right]. \tag{13}$$

We next choose a third constraint in order to solve for the three circuit model elements. Here the choice is optional since neither the real nor the imaginary part has been fixed by (12) and (13). Upon investigation, it is determined that selecting the real parts to be equal at f_l allows reduction of the simultaneous equations to linear equations, whereas selecting the imaginary parts to be equal at f_l produces simultaneous quadratic equations. We therefore set the real parts of the admittance equal at f_l

$$G_l = R/\left[R^2 + (2\pi f_l L)^2\right]. \tag{14}$$

Equations (12) and (14) are now inverted, scaled appropriately, and subtracted to eliminate C as a variable

$$R^2 + (2\pi f_u)^2 L^2 = R/G_u \tag{12'}$$

$$-(f_u/f_l)^2\left[R^2 + (2\pi f_l)^2 L^2 = R/G_l\right] \tag{14'}$$

$$R^2\left[1 - (f_u/f_l)^2\right] = R\left[1/G_u - (f_u/f_l)^2/G_l\right] \tag{15}$$

or

$$R = \left[1/G_u - (f_u/f_l)^2/G_l\right]/\left[1 - (f_u/f_l)^2\right]. \tag{16}$$

Since R is given from (16), it is possible to solve for L in (12)

$$L = \sqrt{\left(R/G_u - R^2\right)}/(2\pi f_u). \tag{17}$$

Next, C is obtained using (13)

$$C = \left\{B_u + (2\pi f_u L)/\left[R^2 + (2\pi f_u L)^2\right]\right\}/(2\pi f_u). \tag{18}$$

Equations (16), (17), and (18) then become the design equations for R, L, and C. Since L is the square root of a potentially negative number, the potential for unrealizable solutions exists.

D. Summary of Model Design Equations

The equations for all of the design models can be derived in a way similar to the derivations illustrated. These equations are summarized here for easy reference.

Series C, R

$$R = R_u \tag{19}$$

$$C = -1/(2\pi f_u X_u). \tag{20}$$

Series L, R

$$R = R_u \tag{21}$$

$$L = X_u/(2\pi f_u). \tag{22}$$

Shunt C, R

$$R = 1/G_u \tag{23}$$

$$C = B_u/(2\pi f_u). \tag{24}$$

Shunt L, R

$$R = 1/G_u \tag{25}$$

$$L = -1/(2\pi f_u B_u). \tag{26}$$

Shunt L, Shunt C, R

$$R = 1/G_u \tag{27}$$

$$C = \left[B_u f_u/f_l - B_l\right]/\left[f_u^2/f_l - f_l\right]/(2\pi) \tag{28}$$

$$L = 1/(2\pi f_u C - B_u)/(2\pi f_u). \tag{29}$$

Series C, Series L, R

$$R = R_u \tag{30}$$

$$L = \left[X_u f_u/f_l - X_l\right]/\left[f_u^2/f_l - f_l\right](2\pi) \tag{31}$$

$$C = 1/(2\pi f_u L - X_u)/(2\pi f_u). \tag{32}$$

Shunt C, Series L, R

$$R = \left[1/G_u - (f_u/f_l)^2/G_l\right]/\left[1 - (f_u/f_l)^2\right] \tag{33}$$

$$L = \sqrt{R/G_u - R^2}/(2\pi f_u) \tag{34}$$

$$C = \left\{B_u + (2\pi f_u L)/\left[R^2 + (2\pi f_u L)^2\right]\right\}/(2\pi f_u). \tag{35}$$

Series L, Shunt C, R

$$G = 1/R = \left[1/G_u - (f_u/f_l)^2/G_l\right]/\left[1 - (f_u/f_l)^2\right] \tag{36}$$

$$C = \sqrt{G/R_u - G^2}/(2\pi f_u) \tag{37}$$

$$L = \left\{X_u + (2\pi f_u C)/\left[G^2 + (2\pi f_u C)^2\right]\right\}/(2\pi f_u). \tag{38}$$

Shunt L, Series C, R

$$R = \left[(f_u/f_l)^2/G_u - 1/G_l\right]/\left[(f_u/f_l)^2 - 1\right] \tag{39}$$

$$C = 1/\sqrt{R/G_u - R^2}/(2\pi f_u) \tag{40}$$

$$L = 1/\left[X_c/\left(R^2 + X_c^2\right) - B_u\right]/(2\pi f_u) \tag{41}$$

where

$$X_c = 1/(2\pi f_u C).$$

Series C, Shunt L, R

$$G = 1/R = \left[(f_u/f_l)^2/R_u - 1/R_l\right]/\left[(f_u/f_l)^2 - 1\right] \tag{42}$$

$$L = 1/\sqrt{G/R_u - G^2}/(2\pi f_u) \tag{43}$$

$$C = 1/\left[B_L/\left(B_l^2 + G^2\right) - X_u\right]/(2\pi f_u) \tag{44}$$

where

$$B_L = 1/(2\pi f_u L).$$

IV. Simplified and Automated Selection of Topologies for Matching Network Synthesis

Topology selection has been a stumbling block in matching network synthesis for the following reasons.

1) Many topologies are available which provide a valid result even after parasitic constraints are applied.

2) Topologies vary in their ability to provide impedance transformations and there is no known way to predict the impedance-transforming capability of a network before it is synthesized.

Given, then, that many topologies are available and that there are no known *a priori* methods for selecting a good topology, the following options were considered in an effort to more efficiently select topologies.

Method 1: Allow (require) the designer to try various topologies and manually select the one which meets his parasitic inclusion and impedance transformation requirements. This has been the traditional approach but is extremely inefficient with respect to the time (and patience) of the microwave designer.

Method 2: Have the computer search through all possible topologies and select out those which meet parasitic inclusion and impedance transformation requirements. This is much more efficient than method 1 since the elimination of invalid topologies is done by the computer. However, the topology search and eliminate process must be done each and every time the designer performs a synthesis, and it still leaves the user to select among the valid topologies that are left.

Method 3: Do an *a priori* study to determine good default topologies for specific combinations of parasitics that need to be included on each side of the network. A good topology would accommodate the existent parasitics and provide a wide range of impedance transformation capabilities. This method provides for the simplest selection of a default topology for the user and would execute in the minimum possible time.

Method 3 was pursued as the best tradeoff for synthesis of matching networks. Therefore, a study was made to determine which topologies provided a wide range of impedance transformation for a given set of parasitics at each end of the matching network. Several general conclusions were drawn from this study.

The first is that the impedance-transforming capability of a matching network is most strongly dependent upon the topology itself and much less strongly dependent upon the frequency response specification. This discovery makes method 3 very workable since default topologies can be selected based upon the requisite parasitic inclusion requirements without regard to the specific frequency response specification.

An illustration of the fact that the impedance-transforming capabiltiy is mostly dependent upon the topology and not the frequency response is given in Table I. Here, the frequency response is varied from 0 dB/octave to 12 dB/octave slope for three different networks. Note that the impedance transformation capability most strongly follows the topology and not the frequency response.

TABLE I
Example of the Impedance Transformation Range of a Network as a Function of Frequency Response and Topology

	Frequency Response		
	Bandwidth =2.1, Ripple= 1 dB, Minimum Loss= 0 dB		
Network Topology	Slope=0 dB/Octave	Slope=6 dB/Octave	Slope=12 dB/Octave
CS LP LS CP	1:2.0 to 1.18.0	1:2.3 to 1.47.0	1.1.8 to 1.91.0
CP LS LP CS	1:0.067 to 1.0.54	1·0.057 to 1.0.43	1:0 034 to 1·0 55
CP LP CS LP	1:0.34 to 1:2.9	1:0.61 to 1:6.2	1·0 68 to 1·13 3

A second general conclusion is that sufficient flexibility is obtained for matching network topologies without requiring networks any higher than six reactive elements. In fact, fourth-order networks are often quite satisfactory in obtaining the requisite bandwidth, parasitic inclusion capability, and impedance transformation. For automation simplicity, all default topologies were chosen to be sixth-order matching networks.

A listing of the selected default topologies along with their approximate impedance transformation range is given in Table II. These topologies were selected strictly on the criterion of wide impedance transformation range; realizability in distributed form at any particular frequency range was not considered.

V. Improved and Automated Methods of Adjusting the Gain–Bandwidth and Selecting Reflection Coefficient Zeros to Ensure Inclusion of Parasitic Elements

The gain–bandwidth of a synthesis has to be constrained and the reflection coefficients have to be selected (either left half plane or right half plane) properly in order to ensure that existent parasitics can be included into synthesized networks. This can be a tedious manual process to adjust the gain, try all combinations of reflection zeros, etc., especially for a microwave designer unfamiliar with synthesis theory.

The approach taken here is to automate the gain–bandwidth adjustment and reflection zero process in the following way.

1) From a given frequency response specification (set by the user), automatically adjust the gain (if and only if necessary) to ensure parasitic inclusion and save all solutions that meet the parasitic inclusion requirements. This provides a set of several valid solutions that can be quickly stepped through and selected by the user.

2) The method of gain adjustment is a binary search on the gain parameter whereby:

a) A maximum allowable gain is first tested to see if it meets the parasitic requirements (e.g. 1 dB);

TABLE II
DEFAULT TOPOLOGIES WHICH PROVIDE A WIDE RANGE OF IMPEDANCE TRANSFORMATION

Input Parasitic Type	Output Parasitic Type	Default Topology	Number of Elements	Number of Hi Pass	Impedance Range l. to l:
CS	CS	CS LS LP CP LS CS	6	3	0 021 48 0
CS	LP	CS LP LS CS CP LP	6	4	0 23 220 0
CS	LS	CS LS LP CP CS LS	6	3	0 011 48 0
CS	CP	CS LP CS LS LP CP	6	2	0 27 203.0
CS	-	CS LS LP CP CS LS	6	3	0 11 48.0
LP	CS	LP CP LS CS LP CS	6	4	0 0045 4.5
LP	LP	LP CP LS CS CP LP	6	3	0.018 48 0
LP	LS	LP CP LS CS CP LS	6	2	0 0037 5.4
LP	CP	LP CP CS LS LP CP	6	3	0 011 87 0
LP	-	LP CP LS CS CP LP	6	3	0 018 48.0
LS	CS	LS CS CP LP LS CS	6	3	0.021 87.0
LS	LP	LS CS LP CP CS LP	6	4	0.23 248 0
LS	LS	LS CS LP CP CS LS	6	3	0.011 87.0
LS	CP	LS CP CS LS LP CP	6	2	0 18 221 0
LS	-	LS CS CP LP LS CS	6	3	0 011 87.0
CP	CS	CP LP CS LS LP CS	6	4	0 0040 4.3
CP	LP	CP LP CS LS CP LP	6	3	0 011 47.0
CP	LS	CP LS LP CP CS LS	6	2	0 0045 5.4
CP	CP	CP LP CS LS LP CP	6	3	0.011 87.0
CP	-	CP LP CS LS CP LP	6	3	0 0011 87 0
-	CS	LS CS CP LP LS CS	6	3	0.011 87.0
-	LP	LP CP LS CS CP LP	6	3	0 011 87.0
-	LS	CS LS LP CP CS LS	6	3	0.011 87.0
-	CP	CP LP CS LS LP CP	6	3	0 011 87.0
-	-	LP CP CS LS LP CP	6	3	0.011 87.0

```
SPARAMETER DATA USED FOR MODEL :
    f(GHz)    S11MAG     S11ANG     S21MAG     S22MAG     S22ANG
     6.000     0.769    -97.000     2.771      0.486     -48.000
    12.000     0.678   -132.000     2.771      0.564     -71.000

ELEMENT VALUES ARE IN  Ohms  pF  nH

BEST 2-ELEMENT MODEL FOR S 1  1
    CS         R
    0.6231     11.4134
FIT IS EXACT AT Fupper. . . .ERROR AT Flower =          0.613  %
APPROXIMATE WORST CASE ERROR IN dB =                    0.027  dB

BEST THREE ELEMENT MODEL OF SERIES-SERIES or SHUNT-SHUNT TYPE FOR S 1  1
    LS         CS         R
    0.0030     0.6166     11.4134
FIT IS EXACT AT Fupper. . . .ERROR AT Flower =          0.634  %
APPROXIMATE WORST CASE ERROR IN dB =                    0.028  dB

BEST SERIES-SHUNT or SHUNT-SERIES THREE ELEMENT MODEL FOR S 1  1
    LP         CS         R
   11.9350     0.6337     10.8903
FIT IS EXACT AT Fupper. . . .ERROR AT Flower =         17.335  %
APPROXIMATE WORST CASE ERROR IN dB =                    0.694  dB

BEST 2-ELEMENT MODEL FOR S 2  2
    CP         R
    0.1679     123.5758
FIT IS EXACT AT Fupper. . . .ERROR AT Flower =         18.413  %
APPROXIMATE WORST CASE ERROR IN dB =                    0.734  dB

BEST THREE ELEMENT MODEL OF SERIES-SERIES or SHUNT-SHUNT TYPE FOR S 2  2
    LP         CP         R
  -14.9671     0.1561     123.5758
FIT IS EXACT AT Fupper. . . .ERROR AT Flower =          0.003  %
APPROXIMATE WORST CASE ERROR IN dB =                    0.000  dB

BEST SERIES-SHUNT or SHUNT-SERIES THREE ELEMENT MODEL FOR S 2  2
    LS         CP         R
   -0.1614     0.1812     89.6381
FIT IS EXACT AT Fupper. . . .ERROR AT Flower =          1.440  %
APPROXIMATE WORST CASE ERROR IN dB =                    0.062  dB
```

Fig. 3. FET gain and impedance modeling

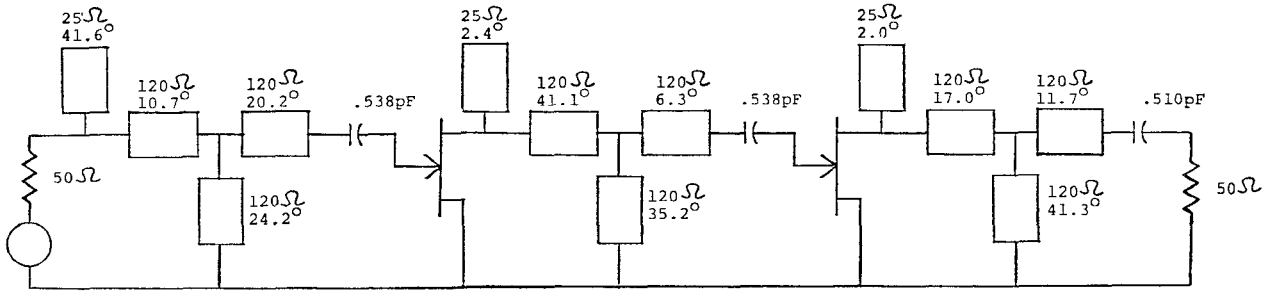

Fig. 4. Gain amplifier. Electrical degrees are at $f_u = 12$ GHz.

b) then half maximum is tested;
c) depending on the results of a) and b), either 1/4 maximum or 3/4 maximum is tested;
d) the process continues until the difference between successive successful tests is sufficiently small (e.g. 0.1 dB).

This method is very efficient because the binary search algorithm converges quite rapidly and because the testing for parasitic inclusion can be obtained with straightforward calculations.

3) The designer is not bothered with the inner workings of the synthesis computations. Rather, the designer specifies requirements such as frequency response, parasitics to be included, and source and terminating resistance and is then presented alternative solutions which can be quickly scanned for selection.

VI. GAIN AMPLIFIER DESIGN EXAMPLE

The data given below pertain to the design example.

AMPLIFIER SPECIFICATIONS: 15 dB ± 2 dB over 6–12 GHz.
TRANSISTOR: The (chip) HP GaAs FET whose parameters are listed in Fig. 3.
TRANSISTOR MODELING: The transistor is shown modeled in Fig. 3 using a computer-aided implementation of the techniques of this paper.
MATCHING NETWORK SPECIFICATIONS:

	Gain Slope	*Ripple*	*Parasitics to be Included*	
Input	6 dB/Oct	.4 dB		FET I/P
Interstage	6 dB/Oct	.4 dB	FET O/P	FET I/P
Output	0	.04 dB	FET O/P	

Figs. 4 and 5 show the analysis of the complete amplifier response. This response is exactly as designed without optimization. Deviations from ideal expectations exist due to the fact that the transistors are not unilateral ($S12 \langle\rangle 0$) and due to the fact that the transmission-line realization is not an exact representation of the lumped design. Overall, the results are a very good first-cut design and could be improved further through optimization.

VII. NOISE FIGURE AMPLIFIER DESIGN EXAMPLE

A single-stage amplifier will be designed to operate over 6–12 GHz with the requirements of minimum noise figure and maximum gain consistent with minimum noise figure. The transistor used is an NEC GaAs FET biased for low-noise operation.

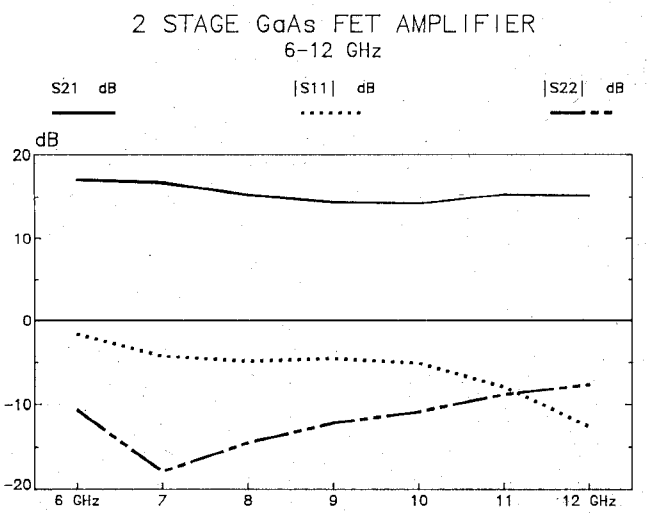

Fig. 5. Analysis of gain amplifier.

```
COMMAND ? FIL-NF
DEVICE FILE NAME ? N700000A
BEST 2-ELEMENT MODEL FOR S 1 1
FOR NOISE MATCHING
CP      R
0.4635 24.2496

COMMAND ? FIL-SP
DEVICE FILE NAME ? N700000A
BEST 2-ELEMENT MODEL FOR S 2 2
CP      R
0.1329   130.4236
```

Fig. 6. Device modeling for noise figure amplifier.

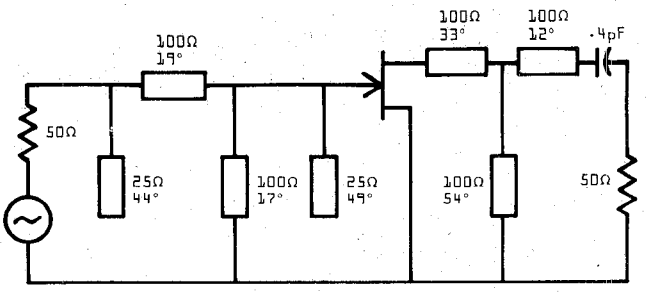

Fig. 7. Noise figure amplifier. Electrical degrees are at $f_u = 12$ GHz.

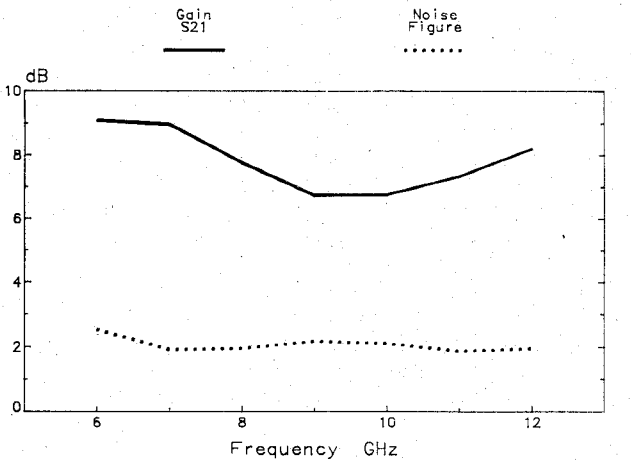

Fig. 8. Analysis of noise figure amplifier.

The requirements are easily translated into specific design specifications for the input and output matching network:

Input Network: Minimum Noise Figure

Output Network: Best Match.

An abbreviated description of the device modeling is shown in Fig. 6 and the completed amplifier and analysis are shown in Figs. 7 and 8.

VIII. Summary

Simplified and improved synthesis techniques coupled with automation of the same provide a powerful and usable tool in the design of wide-band matching networks for microwave amplifiers. The improvements described here, namely, simple and automatable device impedance modeling methods, provision for good default topologies for matching network synthesis, and automated gain–bandwidth adjustment and reflection zero selection, greatly enhance the utility of synthesis as a rapid and accurate design tool for wide-band microwave design.

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